Analog Integr Circ Sig Process (2017) 92:303–314
DOI 10.1007/s10470-017-0994-3

SDTSPC-technique for low power noise aware 1-bit full adder

Preeti Verma[1] · Ajay K. Sharma[2] · Arti Noor[3] · Vinay S. Pandey[4]

Received: 27 October 2016 / Revised: 20 April 2017 / Accepted: 24 May 2017 / Published online: 5 June 2017

Abstract This paper presents a new design named as SDTSPC (Stacked and diode transistor based TSPC) logic for 1-bit full adder to achieve low power noise aware design. Gated transistors are used as stacked transistors from supply to ground path in both sum and carry circuits. One diode connected transistor is placed in series with evaluation transistor to achieve further improved performance in terms of reduced bouncing noise. Analysis is done for power consumption and propagation delay during active and idle mode of operation for both low (25 °C) and high (110 °C) die temperature. Comparing SDTSPC with recently proposed static 1-bit hybrid full adder we get more than 90% improvement in PDP while 30.7% improvement when compared to dynamic TSPC based 1-bit full adder. Corner analysis verifies that our design has the least effect of process exaggeration on PDP and with varying temperature and supply voltage this design keeps lowest value of current among other techniques. SDTSPC design has reduced ground and supply bounce noise. The proposed design is also compared with several previously proposed designs and it is found to have best power delay product (PDP). Further, SDTSPC technique is implemented on 32-bit ripple carry adder as an prolongation of technique.

✉ Preeti Verma
preetiverma@nitdelhi.ac.in

[1] Department of Electronics and Communication Engineering, National Institute of Technology, Delhi 110040, India

[2] Department of Computer Science and Engineering, National Institute of Technology, Delhi 110040, India

[3] School of Electronics, Centre for Development of Advanced Computing, Noida, India

[4] Department of Applied Science, National Institute of Technology, Delhi 110040, India

Keywords Deep submicron · Power consumption · Stacking · Self controlled stacked transistor · TSPC logic

1 Introduction

Feature sizes of the transistors reduces with technology scaling, results in increase of the number of devices and the density in integrated circuits [1–3]. Capacitive coupling increases due to high interconnection density along with high clock frequency [4]. Thus the noise spikes get make the logic malfunction and reduced speed of circuit. Further, by scaling of supply voltage is done, threshold voltage is also to be reduce for maintaining the circuit performance, which increases the leakage current of the device. Thus, as the technology is advancing, we need to find solution to the problem of high power consumption during active as well as in idle mode of operation. Due to reduced device count and high speed, dynamic logic has been broadly used in many applications such as digital signal processors, memory and microprocessors [5].

The performance of dynamic circuits degrades drastically in the cascaded mode of operation. True single phase clock (TSPC) logic design utilizes single clock signal (ø) without inverting it. This has no clock skew problem because the inverted clock is nowhere used in the logic. Consequently, for dynamic pipelined operations high clock frequencies can be achieved.

The TSPC has an additional advantage that logic functionality can be embedded into the latch and due to this delay related to the latches reduces. The TSPC CMOS technique fits not only to dynamic but also to static CMOS circuits. The concept can be applied to any digital CMOS logic circuit.

In this paper, we address the problem of designing low noise energy efficient dynamic TSPC logic for digital CMOS circuits. We name the proposed design as SDTSPC (Stacked diode transistor based TSPC) logic. In order to accomplish the low energy consumption, stack effect in supply to ground path is used and for noise minimization self controlled NMOS transistor is placed in series with evaluation transistor.

We perform extensive experiments on the proposed design through simulation run and compare their results with other standard dynamic circuit design techniques namely dynamic logic and TSPC logic. Further the comparison of proposed design is done with other thirteen existing approaches. It is important to note that many techniques have been proposed to design a dynamic TSPC logic. However, most of these designs have not addressed noise problem and sizing of evaluation transistor.

Our contribution is summarized as follows:

- A energy and noise aware TSPC design to overcome the drawback of dynamic circuits.
- Efficient selection of design by considering clock skew and cascading problem.
- Simulation of proposed SDTSPC design for active and standby power consumption at low and high die temperatures.
- Noise and corner analysis to find the robustness of the proposed design against the PVT variations and noise generating.
- Comparison of simulation results to demonstrate the superiority of proposed design over the existing designs.
- Application of proposed design in 32-bit ripple carry adder.

The rest of the paper is organized as follows. The related work is presented in Sect. 2. The main elements are discussed in Sect. 3, which includes stacking and self controlled transistor study. The proposed design and the simulation results are presented in Sects. 4 and 5 respectively, Sect. 6 presents the application of proposed design and Sect. 7 concludes the paper followed by acknowledgment and references.

2 Related work

Addition is an obligatory operation that is crucial to process the fundamental arithmetic operations. It is used extensively in many VLSI design paradigms and is far the most frequently used operation in general-purpose system and in application specific processors. The refinement in performance of adder results into the improvement of the performance of the system.

The conventional static CMOS full adder consist of 28 transistors and no clock signal [6]. Another smart design in complementary mode is mirror adder [7], which has approximately same power consumption and transistor count (as that of [6]) but the propagation delay is smaller. CPL has good voltage swing restoration and uses 32 transistors [8, 9]. The disadvantage of CPL is high transistor count, high switching activity of intermediate nodes and input overloading. This design is beautifully improved in terms of voltage degradation and transistor count in [10], but the drawback of high power consumption and slow speed still exist. In [11], impact of slope of clock pulse has been studied and based on that quantitative limits and requirement of clock buffer is presented. Authors of [12] have presented low power TSPC based domino logic design. They have also demonstrated a keeper design for charge sharing problem but noise issue is not considered. One more design is presented by the author of [13], based on multithreshold CMOS technique.

Further many more designs are proposed with one or the other tradeoffs. The conventional static CMOS designs cannot provide a high speed digital design, so to achieve fast digital designs dynamic logic circuits are to be used. Dynamic full adder [14] circuit consisting of two precharge transistors. True single phase clock (TSPC) circuits offers fully pipelined high speed digital circuits using single clock signal [15–18]. The true single phase dynamic CMOS circuit technique uses only one clock signal hence no clock skew problem. TSPC logic is more robust in characteristics and implementations [19].

Our proposed SDTSPC design has the following advantages over the existing ones.

- Low energy consumption and reduced switching noise.
- Faster than other dynamic circuit design styles.
- During precharge mode, there is no charge sharing problem at dynamic node.
- Supply and ground bounce is reduced, so as the losses.
- Proposed design is robust against process corner variations as compared to other designs.

3 The main elements

3.1 Stack effect and self bias transistor

The basic idea using stack concept is that “a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path”. When deep submicron MOS transistors operate in the sub threshold region, the standby drain current is exponentially dependent on the gate-source voltage. Therefore, in CMOS logic

circuits, even when gate to source voltage $V_{gs} = 0$, a DC leakage current still exists. Figure 1 shows the stacking of transistors. Most of CMOS logic circuits are composed of series–parallel combination networks of MOS transistors. The analysis of the standby current of stacked MOS transistors with $V_{gs} = 0$ is essential to measure the DC power of deep submicron CMOS circuits [20].

$$I_{S1} = I_0 \exp(CV_{ds3}/nV_T) \exp(-V_{th0}/nV_T) \exp(\eta V_{DD}/nV_T)$$
$$= 1.8I_0 \exp(-V_{th0}/nV_T) \exp(\eta V_{DD}/nV_T) \text{ and } I_{S2} = 1.8I_0 e$$

$$I_{S3} = I_0 \exp(-V_{th0}/nV_T)$$

Thus, I_{s1}: I_{s2}: I_{s3} = 1.8 exp(η V_{DD}/n V_T): 1.8:1. Where I_{si} (i = 1, 2, 3) is leakage current for stacked MOS transistors, V_{ds2} and V_{ds3} are the voltages across transistor M_2 and M_3 respectively.

The above equation shows that as the number of stacked transistors is increasing, leakage current is decreasing. Figure 2 shows, self bias transistors in which gate and drain are tied together as a single node. The beauty of self bias transistors is that, they do not require any external control circuitry, the control signal is generated within the circuit itself.

3.2 Sizing of stacked/diode transistor

Since Gate and Drain are shorted (Fig. 2(a)), the following saturation condition always holds [21]:

$$V_{ds} > V_{gs} - V_{th}$$

where V_{ds} is drain to source voltage, V_{gs} is gate to source voltage and V_{th} is the threshold voltage of MOS transistor.

This means that once $V_{ds} > V_{th}$, the transistor begins to conduct and enters in saturation region. In saturation region the current (after substitution $V_{gs} = V_{ds}$ for diode mode) is given as:

$$I_{ds} = \mu C_{ox} \frac{W}{2L} (V_{ds} - V_{th})^2;$$

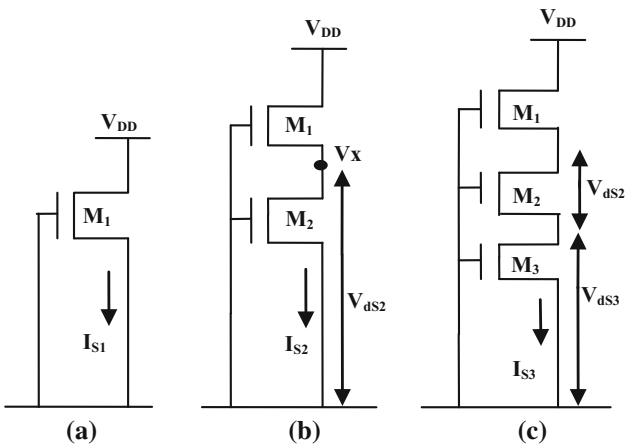

Fig. 1 **a** One NMOS, **b** two stacked NMOS transistors, and **c** three stacked NMOS transistors with $V_{gs} = 0$

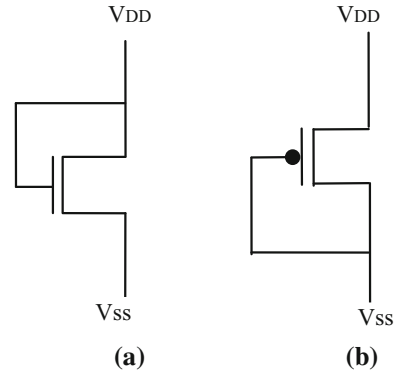

Fig. 2 **a** NMOS self-bias transistor **b** PMOS self-bias transistor

where μ is mobility, C_{ox} is oxide capacitance, W and L are width and length of the channel.

The equivalent resistance of this MOS transistor is:

$$R = \frac{V_{ds}}{I_{ds}} = \frac{2L}{W} \frac{1}{\mu C_{ox}} \frac{V_{ds}}{(V_{ds} - V_{th})^2}$$

Thus, the equivalent resistance can be controlled by changing the dimensions of the transistor (W, L). However, this resistance is not constant, it also depends on the applied bias voltage.

Figure 3 shows the variation of total current for a series of one NMOS transistor and one NMOS diode transistor.

Varying the bias voltage of diode transistor changes the current drawn from the supply voltage. The resistance reduces with positive body bias and reduces with negative body bias Thus we have higher current at positive body bias voltage. On the positive side there are many application which do not require precision in resistances. For the consistency of analysis, the bias voltage is taken as zero. The minimum width for NMOS is taken as 400 nm and for PMOS it is taken as 1200 nm. Sizing of transistors is done to maintain the required amount of current and to fulfil the condition of appropriate charging and discharging of the capacitances.

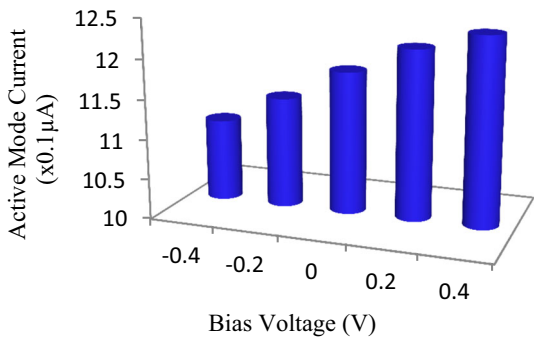

Fig. 3 Active mode current variation of a diode connected NMOS in series to another NMOS transistor with body using cadence virtuoso

4 SDTSPC technique (proposed)

In TSPC logic when clock signal ø is at logic low value, the output node is precharged to logic high value (V_{dd}) through the PMOS precharge transistor. Evaluation phase occurs when the clock signal rises from low logic to high logic value and valid output is generated by the latch.

A new adder cell is presented in Fig. 4. The proposed circuit effectively reduces the total power consumption and idle mode power consumption also. The key idea behind the target approach is reduction of power consumption by the use of effective stacking of transistors from supply voltage to ground path. The observation is based on [20, 22], in which it is shown that a state with only one stacked transistor is far more leaky than a state with more than two transistors off in the stack from supply to ground path. Diode footed transistor is connected in series with evaluation transistor for further improvement of noise and power consumption [23].

Proposed circuit consist of two PMOS precharge transistors M_{pc1} and M_{pc2}, one evaluation NMOS transistor M_E, four gated leakage control transistors out of which two are NMOS (M_{n1}, M_{n2}) and two are PMOS (M_{p1}, M_{p2}) transistors. One NMOS transistor M_D is placed as a diode connected pattern (gate terminal of the transistor connected to the drain terminal of the transistor)) in series with the evaluation network. Introduction of gated leakage control (GLC) transistors and diode connected transistor creates stack effect and thus reduces the power consumption.

The advantage of transistor M_D is reduced bouncing noise during evaluation phase. As during precharge to evaluation mode transition the transistor M_E turns on first, then transistor M_D turns on when the voltage at node N_3 is up to the threshold voltage of transistor M_D and thus reduced the sudden current surge. This makes the circuit less noisy. Another advantage of proposed technique is that no extra control circuit is required to control the operation of leakage control transistors. Further the reduction in power consumption is obtained connecting the source terminal of latch NMOS (towards ground) to the node N_E. By doing this leakage is reduced as the evaluation transistor id off during precharge mode so there will be no current from latch transistor during precharge mode and during evaluation current surge will be reduced.

During precharge mode, precharge transistors (M_{PC1}, M_{PC2}) are turned on so the voltage at node P_1 and P_2 goes

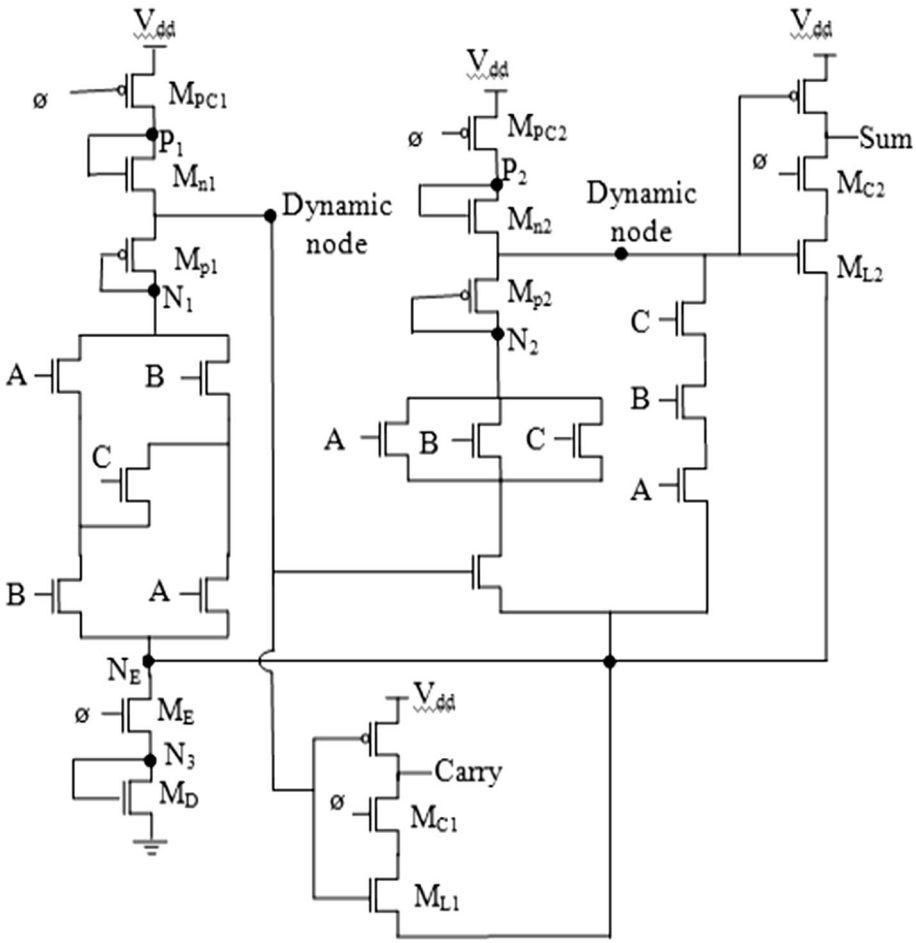

Fig. 4 Proposed SDTSPC full adder

high, thus the gated leakage control transistors Mn1 and Mn2 are turned on and precharges the output node. During this phase gated leakage control transistors M_{p1} and M_{p2} are turned off as the evaluation transistor is off, voltage at node N1 and N2 reaches to high value resulting in an increased stack of transistors.

During evaluation mode, precharge transistor is off so the GLC transistors are also off thus creating an stack of transistors from supply to ground path. Depending upon the input values voltage level at node N_1 and N_2 goes low or remains high. If it goes low transistor Mp1 and Mp2 will get turned on and provides the evaluation path for the charge stored at the dynamic node. Thus during evaluation phase, if inputs are such that there is no discharge path towards ground then GLC transistors increase the stack effect as they are off and thus reduces the power consumption of the device. Thus the proposed circuit is low power consuming and less noisy at the same time there is small increase in delay. The proposed technique can be applied to any circuit's critical path from supply voltage to ground for the reduction of power consumption.

Table 1 Sizing of transistors (nm)

Transistor	Standard design	Proposed design
Precharge PMOS	1080	1080
Latch PMOS	800	800
Latch NMOS	400	400
Diode NMOS	–	400
Diode PMOS	–	1080

5 Simulation results and analysis

Simulation is performed using cadence specter 180 nm PDK BSIM3V3 process models. Dynamic full adder, TSPC full adder and modified TSPC full adder circuits are simulated using Supply voltage 1.8 V, clock frequency 500 MHz, load capacitance is taken as 1 fF at both sum and carry outputs. For measuring active power consumption, a clock pulse of 2 ns is applied on all possible input combinations. Analysis is done for both low (25 °C) and high temperature (110 °C). PDP analysis is done for active mode as well as idle mode operations. Sizing of diode transistor is done to obtain the minimum possible delay. The channel length is taken as 180 nm and minimum width of NMOS transistor is taken as 400 nm for both conventional and proposed design. The logic transistors for both the circuits have standard sizing. The size of other transistors for standard and proposed circuit design are given in Table 1.

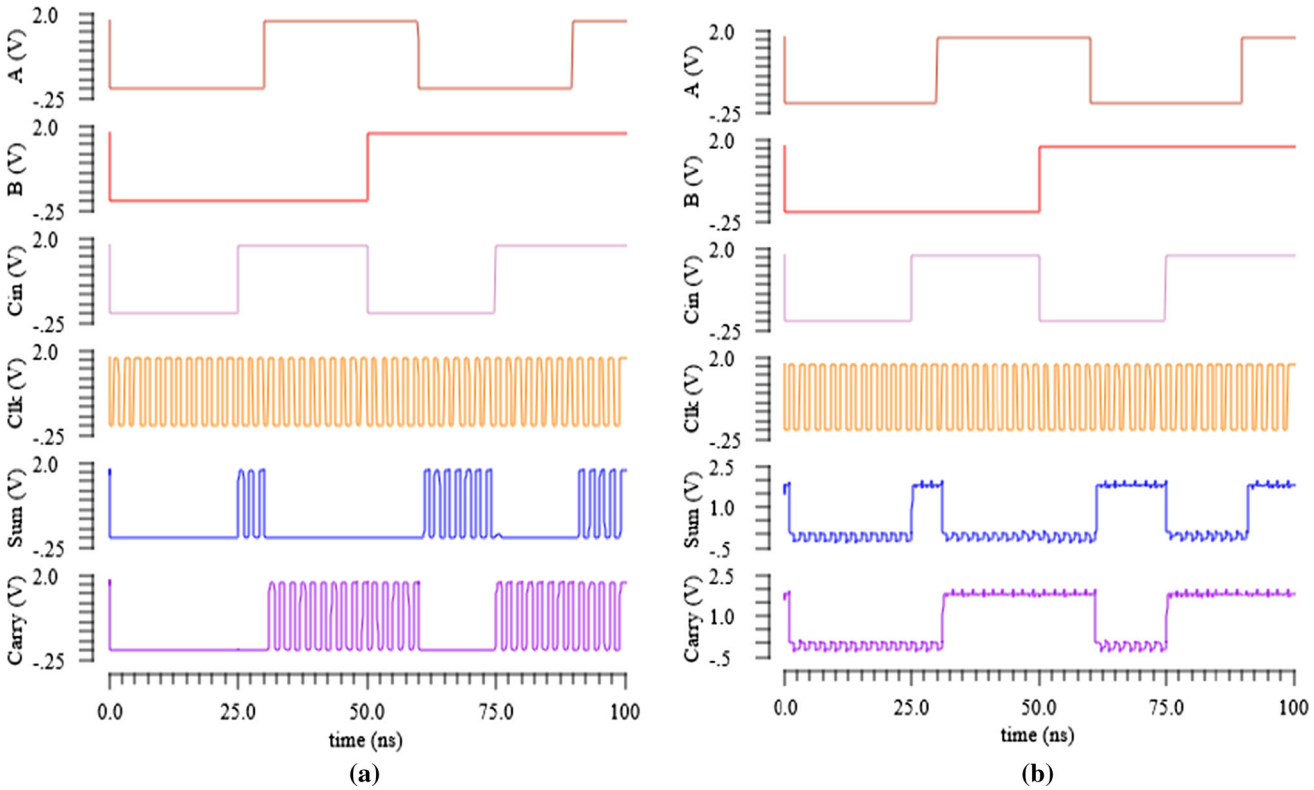

Fig. 5 Transient characteristics of **a** standard dynamic adder, **b** proposed SDTSPC adder

5.1 Active mode power consumption and delay at low (25 °C) and high die temperature (110 °C)

For every switching power consumption is given as: Supply voltage (V_{DD}) * Current (I).

If input logic is high, because of pulses in evaluation phase the switching of buffer output will be regular same as the clock switching. Therefore large current flows into the buffer and results in increased power consumption. Figure 5(a), (b) shows the input and output waveforms of standard dynamic adder and proposed SDTSPC adder respectively.

In both the figures the first and second waveform data inputs (A, B), third is carry input (Cin), the fourth waveform is clock signal, fifth and sixth waveforms are sum and carry output respectively. It can be seen from the figure, that the sum and carry outputs of standard dynamic full adder contains a lot of noise. When outputs sum and carry of basic dynamic full adder is one, it gets ON and OFF with each clock switching. On the other hand proposed full adder circuit, does not have the switching pulses in the outputs (sum and carry), thus resulting in low power noise aware faster design. The proposed SDTSPC technique produces slightly weak logic levels at the output sum waveform around 1.79 V for logic high and 30.876 mV for logic zero. Similarly for output carry in waveform logic one is around 1.79 V and the logic zero is approximately 51.98 μV.

Figure 6 represents the variation of total current for fifty clock cycles with temperature variation, for basic dynamic design, TSPC and proposed SDTSPC full adder circuits. We can find that the proposed design has smaller current for whole temperature range as compared to other design's current i.e. lower power consumption. Power, delay and power delay product (PDP) for dynamic FA, TSPC FA and proposed SDTSPC FA is tabulated in Table 2.

For proposed SDTSPC design, 73 and 78.8% reduction in PDP is obtained as compared to standard dynamic full adder at low (25 °C) and high (110 °C) die temperatures respectively. Similarly, 28.3 and 15.5% reduction PDP is obtained as compared to standard TSPC full adder at low and high die temperatures respectively. PDP variation is shown by bar chart in Fig. 7 and it can be concluded, that the proposed design has the minimum PDP at both low and high temperature. Switching power reduction was initially achieved by supply voltage scaling. It is an effective method for switching power reduction because of the quadratic dependence of the switching power on the supply voltage [24]. Figure 8 shows the variation of total current for fifty clock cycles, drawn from supply voltage with respect to the variation in supply voltage. We can see that

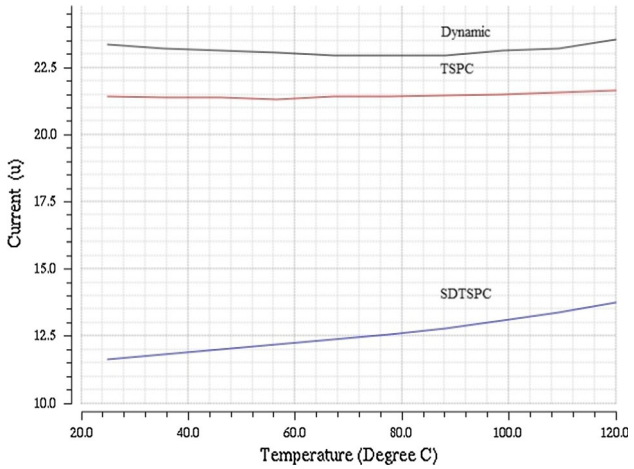

Fig. 6 Variation of total current with temperature for dynamic, TSPC and SDTSPC full adders

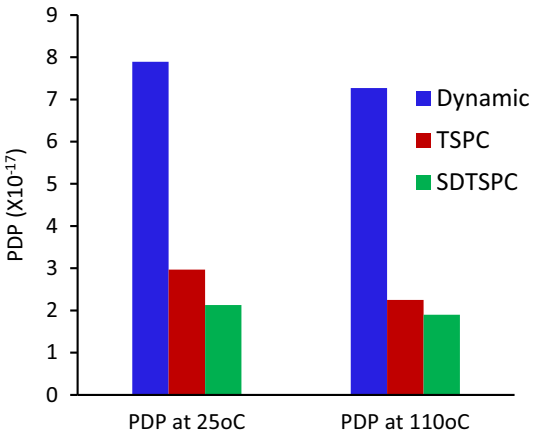

Fig. 7 PDP comparision of proposed design with conventional design

Table 2 Power, delay and PDP with at low and high die temperatures

FA design	25 °C			110 °C		
	Power ($\times 10^{-7}$)	Delay (ps)	PDP (10^{-17})	Power ($\times 10^{-7}$)	Delay (ps)	PDP (10^{-17})
Dynamic [14]	8.28	95.4	7.89	8.43	86.24	7.27
TSPC [19]	7.70	38.7	2.97	7.76	29.05	2.25
SDTSPC	4.02	53.1	2.13	4.15	46.65	1.9

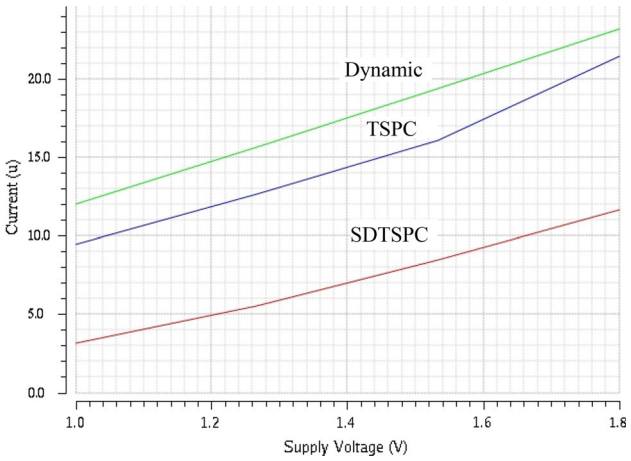

Fig. 8 Variation of total current with supply voltage for dynamic, TSPC and SDTSPC full adders

Table 3 PDP at different supply voltages

Voltage (V)	PDP (10^{-17})		
	Dynamic [14]	TSPC [19]	SDTSPC
1.8	7.23	2.91	2.11
1.6	6.84	2.09	1.44
1.4	6.90	1.55	0.92
1.2	6.75	1.10	0.52
1.0	6.80	1.84	0.26

the current rises with rising value of supply voltage and thus the power consumption too but we get lowest current with proposed design for any value of supply voltage.

Table 3, shows the numerical values of the PDP with supply voltage variation. 87, 36.7 and 5.96% reduction in PDP is found for proposed SDTSPC, TSPC and dynamic adder respectively for supply voltage reduction from 1.8 to 1.0 V.

5.2 Leakage power consumption in idle mode at 25 and 110 °C

Clock signal is high during idle mode of operation, thus the precharge transistor is turned OFF. During idle mode voltage at dynamic node depends upon the inputs of the circuit. To find the leakage current during idle mode two input conditions are taken with clock signal high for long duration. First condition is when dynamic node voltage is high, i.e. all inputs are low and other one is when dynamic node voltage is low, i.e. all the inputs are at logic high. In idle mode the leakage power consumption of the proposed design is tabulated in Table 4.

Comparing dynamic FA and proposed full adder, 56.7 and 56.3% saving in leakage power consumption with all inputs set to logic low value and 13.3 and 22.7% saving with all inputs set to logic high at low and high temperature respectively. Similarly, comparing TSPC FA and proposed FA, 30.2 and 18% saving for low inputs and 12.2 and 16% saving for high inputs at low and high temperature respectively. Thus the proposed design works well at low as well as high temperature.

Table 4 Leakage power consumption during idle mode

Technique	Power (leakage) nWatt			
	All inputs low		All inputs high	
	25 °C	110 °C	25 °C	110 °C
Dynamic [14]	23.61	28.16	24.92	25.63
TSPC [19]	14.50	15.01	24.61	23.62
SDTSPC	10.12	12.30	21.60	19.81

5.3 Corner analysis

The corner tool confer a suitable way for measuring circuit performance using a set of parameter values that constitute the utmost variations in the process. The simulation which takes these variation into consideration will differ from each other. There are five probable process corners: There are therefore five possible corners: Nominal–Nominal (NN), Slow–Slow (SS), slow–fast (SF), Fast–Slow(FS), Fast–Fast(FF). Three corners (NN, FF, SS) effect both type of devices evenly and called as even corners. The other two corners (FS, SF) are cause of concern and termed as skewed corners. With these two corners one type of transistor will switch faster than the other one. So we need to find the tolerance of design with process variations. Figure 9 clearly shows that the proposed SDTSPC full adder circuit shows best result when it is compared with the different corner cases. Variation of PDP for proposed SDTSPC design is minimum with all process corner variations.

Table 5 presents the numerical data obtained using cadence virtuoso for all designs in each corner variation. We found that the proposed circuit shows the best PDP performance under differences process inaccuracies, temperature and other parameter variations. So, the proposed design is more robust against process variations as compared to standard dynamic and TSPC designs.

5.4 Noise analysis

During switching, high current (I) pulses in supply and ground level cause the variation in ground and supply levels. Thus the ground and supply voltages deviate from their nominal values. This is typically termed as switching

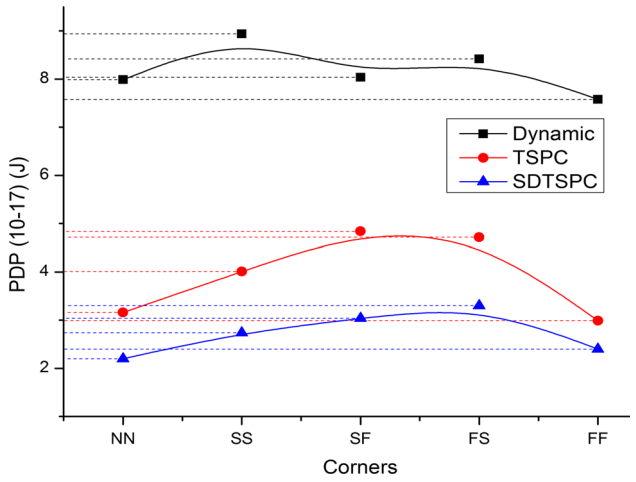

Fig. 9 PDP variation for different process corners

Table 5 PDP of dynamic, TSPC and SDTSPC full adder

FA circuit	PDP ($\times 10^{-17}$)				
	NN	SS	SF	FS	FF
Dynamic [14]	7.94	8.94	8.04	8.42	7.58
TSPC [19]	3.16	4.01	4.84	4.72	3.66
SDTSPC	2.20	2.74	3.04	3.30	2.40

noise/bouncing noise or ΔI noise [25]. Dynamic logic is more sensitive to noise as compared to static logic. However, the noise can be reduced by utilizing several methods. In this paper we have applied the method of step charging and discharging of the node capacitance by the use of self biased transistors. This results in the reduction of ground and supply bouncing noise in TSPC logic.

The analysis of switching noise is done for both standard design and propose design. Figure 10(a), (b) respectively depict the supply bounce and ground bounce voltage for both standard and proposed full adder circuits. In Fig. 10(a), (b), y-axis represents the supply bounce (Vvdd) in volts and ground bounce (Vvgnd) voltage levels in millivolts respectively.

The numerical values of ground bounce and supply bounce voltage levels are tabulated in Table 6. The noise analysis is done for all input combinations (000,001,……..,111) at clock frequency 500 MHz. The bouncing noise modeling is done by RLC modeling. For noise analysis, the typical value of inductance (L), resistance (R) and capacitance (C) is taken as 7 nH, 0.6 Ω and 4 pF respectively. It is found from observation and calculation that the proposed SDTSPC FA circuit has smaller values of ground as well as smaller supply bounce voltage levels. For proposed design, the maximum supply bounce and ground bounce is lowered by 7 and 5.06 mV respectively. As compared to standard design, 39.4 and 42.8% improved peak value (IPV) difference is obtained, respectively for supply bounce noise and ground bounce noise.

CMOS devices also have small amount of thermal and flicker noise. The flicker noise corner is approximately constant, falling in the range of 500 kHz to 1 MHz for submicron devices. While the thermal noise is flat for approximately 100 THz, dropping at higher frequencies [26, 27]. Figure 11 shows the output noise variation with frequency for standard TSPC full adder and proposed SDTSPC full adder. Lower values of output noise are obtained as compared to conventional design.

5.5 Comparison with other techniques

With a target to minimize both power consumption and delay of the circuit, the energy consumption i.e. the PDP has been minimized for the proposed design. It is observed that the power consumption can mainly be minimized by mainly sizing the transistors of the latch circuit and the leakage control transistors inserted at the dynamic node of sum and carry circuit while the delay can be improved by sizing the diode connected transistor below the evaluation transistor. Power delay product of proposed SDTSPC design along with existing designs of full adders are given in Table 7. Because of reduction in power consumption and high speed of TSPC dynamic logic, the PDP of proposed design is significantly improved as compared to other designs.

The PDP variation of proposed design and existing designs is shown in Fig. 12. From this we can see that the proposed design has the minimum PDP as compared to other designs. Comparing SDTSPC with recently proposed static 1-bit hybrid full adder we get more than 90% improvement in PDP while 30.7% improvement when compared to dynamic TSPC based 1-bit full adder.

6 Application to 32-bit ripple carry adder

To add N-bit number, N-Full adder circuits can be cascaded in parallel. Figure 13 shows a 32 bit ripple carry adder, that consist of 32 one-bit full adders is implemented as an prolongation of proposed SDTSPC full adder. It is called ripple carry adder, because the carry bit at each stage gets rippled into next stage. For a ripple carry adder, the worst case delay is when generated carry at least significant bit place propagates to the most significant bit position.

The carry is used at the last stage to generate the sum. The delay depends upon the number of bits in the input and

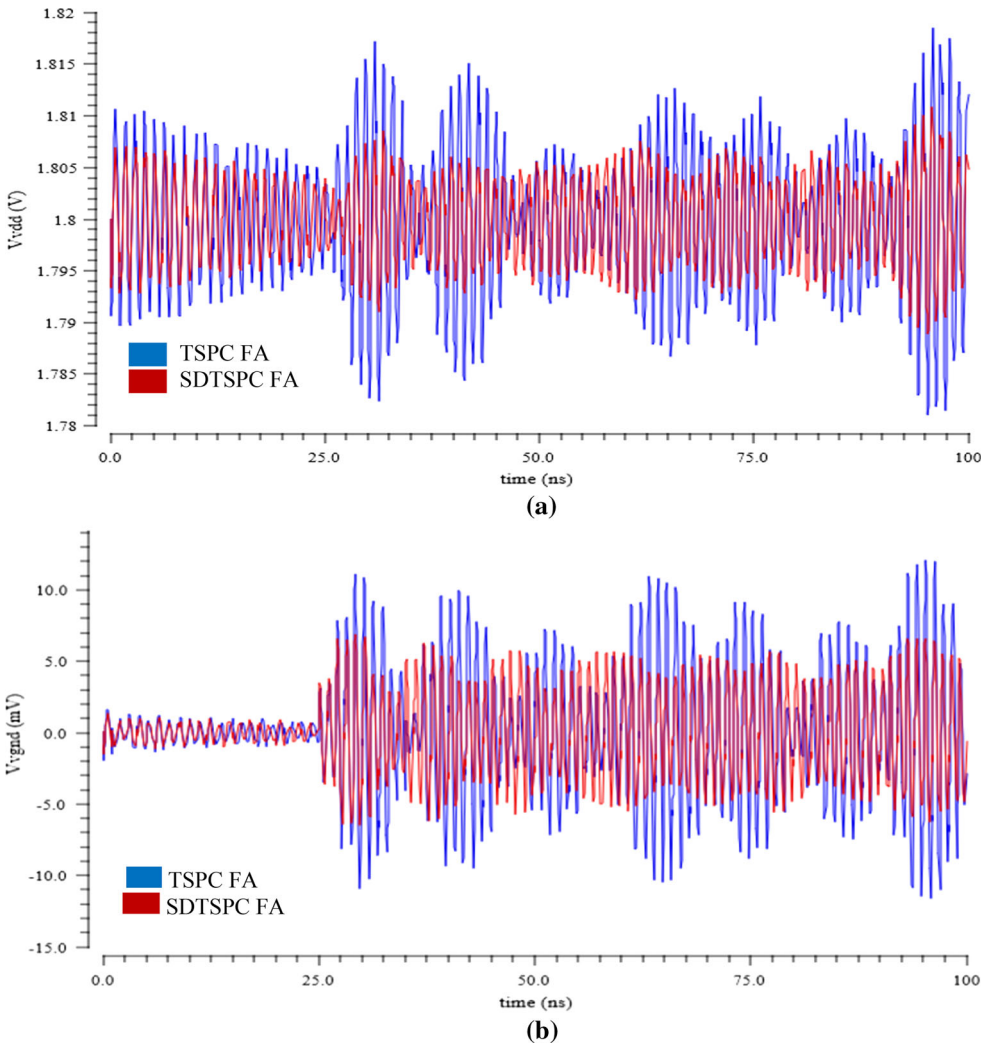

Fig. 10 **a** Supply bounce noise (Volts) **b** ground bounce noise (mVolts)

Table 6 Noise voltage levels of standard and proposed FA

Noise	FA circuit	Maximum peak (Max_p)	Minimum peak (Min_p)	Difference in peak values ($D_p = Max_p - Min_p$)	IPV difference (%)
Supply bounce (V)	Standard design	1.819	1.781	0.038	39.4
	Proposed design	1.812	1.789	0.023	
Ground bounce (mV)	Standard design	12.07	−11.46	23.53	42.8
	Proposed design	7.01	−6.44	13.45	

is approximately given as $T_{adder} \approx (N-1)T_{carry} + T_{sum}$ where T_{carry} and T_{sum} is the delay to propagate the carry from least significant bit to most significant bit and sum respectively.

The performance analysis of the 32 bit ripple carry adder is carried out at 500 MHz and supply voltage 1.8 V for 180 nm BSIM3V3 process models. Dynamic power consumption and carry propagation delay is found to be 12.96 μW and 1.67 ns.

7 Conclusion

In deep submicron dynamic logic designs both the dynamic as well as idle mode power consumption should be reduced along with the suppression of noise. Therefore, a low power and less noisy 1-bit full adder has been proposed utilizing gated leakage control transistors at dynamic nodes and a transistor in diode configuration in series with evaluation transistor.

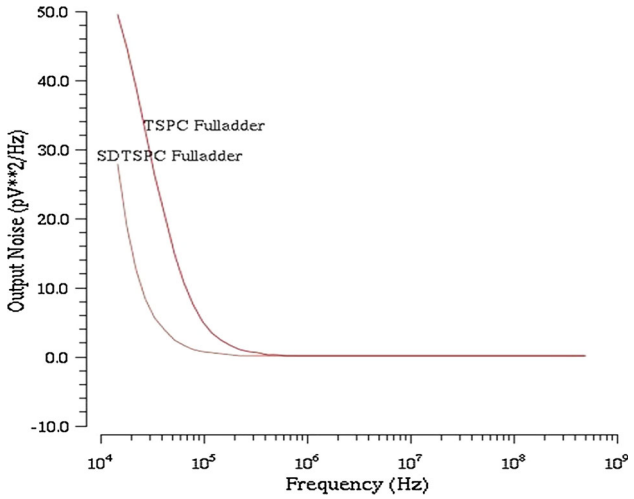

Fig. 11 Output noise of standard TSPC FA and proposed FA using cadence virtuoso

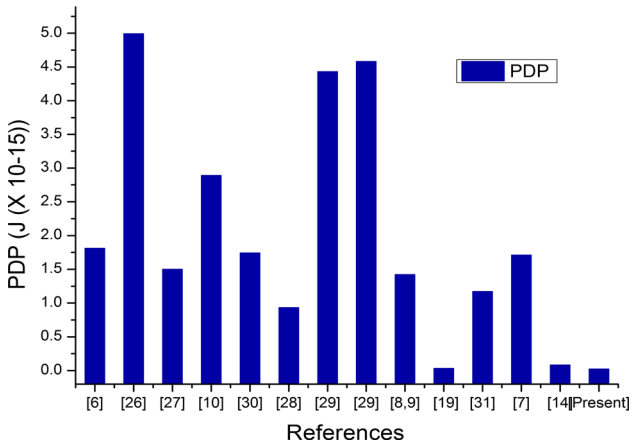

Fig. 12 PDP of existing and proposed designs (on logarithmic scale)

Table 7 Comparison with existing designs

Design	PDP	References
C-CMOS	1.81E−15	[6]
24T	4.99E−15	[28]
FA_Hybrid	1.50E−15	[29]
TGA FA	2.89E−15	[10]
HPSC	1.74E−15	[32]
Hybrid 1bit FA	9.31E−16	[30]
FA-DPL	4.43E−15	[31]
FA-SR-CPL	4.58E−15	[31]
CPL	1.42E−15	[8, 9]
TSPC FA	3.04E−17	[19]
Majority based FA	1.17E−15	[33]
Mirror	1.71E−15	[7]
Dynamic	8.01E−17	[14]
SDTSPC	2.20E−17	[Present]

This design can be extended for several applications. The simulation results establishes that proposed full adder offers improved PDP compared with earlier reports. As it utilizes dynamic charge storage concept, it is very fast and tested up to 500 MHz The results show that reduction of active power by 73 and 78.8% is obtained as compared to standard dynamic full adder at low (25 °C) and high (110 °C) die temperatures respectively. 28.3 and 15.5% reduction in PDP is obtained as compared to standard TSPC full adder at low and high die temperatures respectively. Varying the supply voltage from 1.8 to 1.0 V, PDP of TSPC logic reduced by 36.7% while PDP for proposed design reduces by 87.6%. With increasing temperature power consumption increases but the delay decreases and overall we get higher PDP improvement at high temperature. The SDTSPC design shows almost same PDP for all the corner variations. 18–56% reduction in idle mode power consumption is obtained for different inputs and temperature. As compared to standard FA, the proposed FA design achieves 39.4 and 42% improvement in peak value difference for supply bounce and ground bounce noise respectively.

An analysis of overall results and comparison with already proposed designs identifies the proposed technique as the best among other reported designs. The proposed design is also used to implement 32 bit ripple carry adder. This technique can be used for ultra low power applications such as microprocessors, memory elements, signal processing units etc.

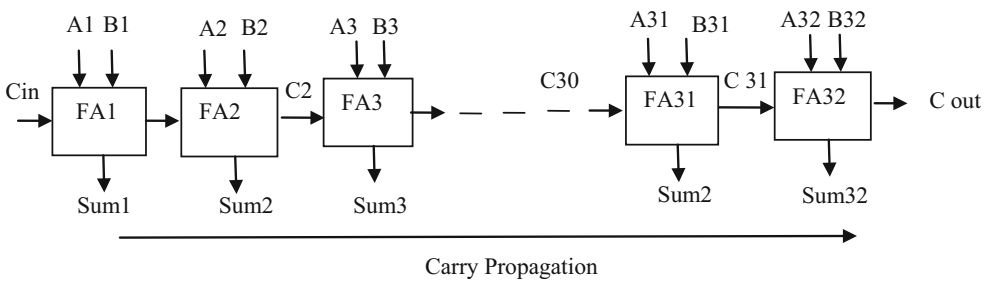

Fig. 13 32-bit ripple carry adder

Acknowledgements This work has been carried out under the project of special manpower development program for chips to system design and funded by Ministry of Communications and information Technology, Government of India.

References

1. Taur, Y. (2002). CMOS design near the limit of scaling. *IBM Journal of Research and Development, 46*(2/3), 213–221.
2. De, V., & Borkar, S. (2002). Technology and design challenges for low power and high performance. In *Proceedings of the IEEE/ACM international symposium on low power electronics and design* (pp. 163–168).
3. Sery, G., Borkar, S., & De, V. (2002). Life is CMOS: Why chase life after? In *Proceedings of the IEEE/ACM international design automation conference* (pp. 78–83).
4. Hernandez, F. M., Aranda, M. L., & Champac, V. (2006). Noise tolerant improvement in dynamic CMOS logic circuit. *IEEE Proceedings Circuits Devices Systems, 153*(6), 565–573.
5. Yeager, H. L., et al. (2004). Domino circuit topology. U. S. Patent 6784695.
6. Weste, N. H. E., Harris, D., & Banerjee, A. (2006). *CMOS VLSI design: A circuits and systems perspective* (3rd ed.). Delhi: Pearson Education.
7. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2003). *Digital integrated circuits: A design perspective* (2nd ed.). Delhi: Pearson Education.
8. Radhakrishnan, D. (2001). Low-voltage low-power CMOS full adder. *IEEE Proceedings Circuits Devices Systems, 148*(1), 19–24.
9. Zimmermann, R., & Fichtner, W. (1997). Low-power logic styles: CMOS versus pass-transistor logic. *IEEE Journal of Solid-State Circuits, 32*(7), 1079–1090.
10. Chang, C. H., Gu, J. M., & Zhang, M. (2005). A review of 0.18-μm full adder performances for tree structured arithmetic circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 13*(6), 686–695.
11. Larsson, P., & Svensson, C. (1994). Impact of clock slope on true single phase clocked (TSPC) CMOS circuit. *IEEE Journal of Solid State Circuits, 29*(6), 723–726.
12. Tang, F., & Bermak, A. (2011). *Lower-power TSPC based domino logic circuit design with 2/3 clock load*. Amsterdam: Elsevier-ICAEE.
13. Mitra, A. (2014). Designing and analysis of a low power high speed 1-bit full adder cell based on TSPC logic with multi-threshold CMOS. *World Academy of Science, Engineering and Technology, 8*(1), 185–188.
14. A System Perspective, Addison Wesley, 1993. J. Uyemura, CMOS logic circuit design. Kluwer, 1999. ISBN: 0-7923-8452-0.
15. Kang, S. M., & Leblebici, Y. (2003). *CMOS digital integrated circuits, analysis design* (3rd ed.). New York: McGrawhill.
16. Weste, N., & Eshraghian, K. (1994). *Principles of CMOS VLSI design*. Boston: Addison-Wesley.
17. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2004). *Digital integrated circuits* (2nd ed.). Indore: Prentice-Hall of India Private Limited.
18. Ji-Ren, Y., Karlsson, I., & Svensson, C. (1987). A true single-phase-clock dynamic CMOS circuit technique. *IEEE Journal of Solid-State Circuits, 22,* 899–901.
19. Ji-Ren, Y., & Svensson, C. (1989). High speed CMOS technique. *IEEE Journal of Solid State Circuits, 24*(1), 62–70.
20. Gu, R. X., & Elmasry, M. I. (1996). Power dissipation analysis and optimization for deep submicron CMOS digital circuits. *IEEE Journal Solid-State Circuits, 31,* 707–713.
21. Rajavi, B. (2002). Design of analog CMOS integrated circuits. Mc-Graw hill.
22. Katrue, S., & Kudithipudi, D. (2008). GALEOR: Leakage reduction for CMOS circuits. In *15th IEEE international conference ICECS 2008*.
23. Flandre, D., Bulteel, O., Gosset, G., Rue, B., & Bol, D. (2012). Ultra-low-power analog and digital circuits and micro systems using disruptive ultra-low-leakage design techniques. In *ICCDCS*.
24. Bhavnagarwala, A. J., et al. (2000). A minimum total power methodology for projecting limits on CMOS GSI. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 8,* 235–251.
25. Delaurenti, M., Graziano, M., Piccinni, G., & Zamboni, M. (2000). Switching noise analysis framework for high speed logic families. In *IEEE conference* (pp. 524–530).
26. Razavi, B. (2005). Design of analog CMOS integrated circuits. TMH.
27. Lee, T. H. (2004). *The design of CMOS radio frequency integrated circuits* (2nd ed.). Cambridge: Cambridge University Press.
28. Tung, C.-K., Hung, Y.-C., Shieh, S.-H., & Huang, G.-S. (2007). A low-power high-speed hybrid CMOS full adder for embedded system. In *Proceedings of the IEEE conference on design diagnostics electronic circuits systems* (Vol. 13, pp. 1–4).
29. Goel, S., Kumar, A., & Bayoumi, M. A. (2006). Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 14*(12), 1309–1321.
30. Tung, C.-K., Hung, Y.-C., Shieh, S.-H., & Huang, G.-S. (2007). A low-power high-speed hybrid CMOS full adder for embedded system. In *Proceedings of the IEEE conference design diagnostics electronic circuits systems* (Vol. 13, pp. 1–4).
31. Aguirre-Hernandez, M., & Linares-Aranda, M. (2011). CMOS full-adders for energy-efficient arithmetic applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 19*(4), 718–721.
32. Zhang, M., Gu, J., & Chang, C.-H. (2003). A novel hybrid pass logic with static CMOS output drive full-adder cell. In *Proceedings of the international symposium on circuits systems* (pp. 317–320).
33. Navi, K., Moaiyeri, M. H., Mirzaee, R. F., Hashemipour, O., & Nezhad, B. M. (2009). Two new low power full adders based on majority-not gates. *Microelectronics Journal, 40*(1), 126.

Preeti Verma completed B. Tech. in Electronics Engineering in year 2007. She did M. Tech. in Microelectronics and VLSI design from Motilal Nehru National Institute of Technology, Allahabad in year 2011. Currently she is Research Scholar at National Institute of Technology, Delhi. Her area of interest is Integrated circuits, low power CMOS circuit design. She has 2 years of industry experience and 3 years of teaching experience as Assistant professor.

Ajay K. Sharma is working as Director National Institute of Technology, Delhi since October 2013. He received his B.E. in Electronics and Electrical Communication Engineering from Punjab University Chandigarh, India in 1986, M.S. in Electronics and Control from Birla Institute of Technology (BITS), Pilani in the year 1994 and Ph.D. in Electronics Communication and Computer Engineering in the year 1999. His Ph.D. thesis was on "Studies on Broadband Optical Communication Systems and Networks". After serving various organizations from 1986 to 1995, he has joined National Institute of Technology (Erstwhile Regional Engineering College) Jalandhar as Assistant Professor in the Department of Electronics and Communication Engineering in the year 1996. From November 2001, he has worked as Professor in the ECE department and thereafter he has worked as Professor in Computer Science and Engineering from 2007 to 2013 in the same institute. His major areas of interest are broadband optical wireless communication systems and networks, dispersion compensation, fiber nonlinearities, optical soliton transmission, WDM systems and networks, Radio-over-Fiber (RoF) and wireless sensor networks and computer communication. He has published 280 research papers in the International/National Journals/Conferences and 12 books. He has supervised 23 Ph.D. and 52 M. Tech. theses. He has completed two R&D projects funded by Government of India and one project is ongoing. He was associated to implement the World Bank project of 209 Million for TEQIP-I programme of the institute. He has been appointed as member of technical Committee on Telecom under International Association of Science and Technology Development (IASTD) Canada for the term 2004–2007 and he is Life Member of Optical Society of America, USA (LM ID-361253), Computer Society of India, Mumbai, India, (LM-Associate: 01099298), Advanced Computing and Communications Society, Indian Institute of Science, Bangalore, India, (L284M1100306), SPIE, USA, (ID: 619838), Indian Society for Technical Education (I.S.T.E.), New Delhi, India, (LM-11724), Fellow The Institution of Electronics and Telecommunication Engineers (IETE), (F-224647).

Arti Noor is currently working with Centre for development of advanced computing, Noida. She has more than 24 years of R&D experience in the field of VLSI design and technology characterization, VHDL and computer programming, and speech synthesis. She obtained her Ph.D. (Electronics and communication Engineering) in 1990 from Banaras Hindu University, Banaras. She started her career from CEERI, Pilani. She was also involved in various research development activities in CEERI, Pilani and in CDAC, Noida. She worked on many consultancy projects for ISRO Bangalore, IIT Delhi, ISAC Bangalore, and VSSC Trivandrum.

Vinay S. Pandey is working as Assistant professor at National Institute of Technology, Delhi. Completed his M. Sc. and Ph.D. from IIT BHU in year 2000 and 2006 respectively. His research interest is in the area of CMOS VLSI design, MHD simulations, Nonlinear plasma theory, Non-uniform transmission lines. He has research experience of Physical research Laboratory (Department of pace, Government of India), World Class University (WCU) Project-under the collaboration of KAS/JAXA and NASA, at School of Space Research, Kyung Hee University, South Korea. He is also the referee's of various National and International journals such as Journal of Plasma Physics: Cambridge University Press, Astrophysics and Space Science: Springer, Indian Journal of Physics: Springer etc.